

文章编号 1004-924X(2009)06-1379-06

具有自检测功能的闭环加速度计接口电路设计

刘云涛^{1,2}, 尹亮¹, 陈伟平^{1,3}, 吴群¹

- (1. 哈尔滨工业大学 MEMS 中心, 黑龙江 哈尔滨 150001;
2. 哈尔滨工程大学 信息与通信工程学院, 黑龙江 哈尔滨 150001;
3. 微系统与微结构制造教育部重点实验室, 黑龙江 哈尔滨 150001)

摘要: 为了改善机电系统(MEMS)电容式加速度计的噪声特性, 提出了一种基于开关电容的低噪声闭环接口电路。该电路采用电荷积分器作为前级预放大装置, 对寄生电容不敏感, 而且具有非常低的噪声。采用相关双采样(CDS)技术消除了 $1/f$ 噪声和运算放大器失调电压的影响。同时, 为了改善系统的动态响应特性, 反馈部分采用积分电路, 提高了系统阻尼比和响应速度。利用电荷泻放通道实现了自检测功能。采用 $0.5\ \mu\text{m}$ CMOS工艺完成了版图设计, 仿真结果表明, 系统灵敏度为 $0.115\ \text{V/g}$, 非线性度 $<0.12\%$, 可检测的最小加速度为 $20\ \mu\text{g}$, 自检测输出与自检测电压成正比。

关键词: 加速度计; 闭环控制; 自检测; 开关电容; 接口电路

中图分类号: TH824.4 **文献标识码:** A

Design of interface circuit of closed-loop accelerometer with self-test function

LIU Yun-tao^{1,2}, YIN Liang¹, CHEN Wei-ping^{1,3}, WU Qun¹

(1. MEMS Center, Harbin Institute of Technology, Harbin 150001, China;

2. College of Information and Communication Engineering, Harbin Engineering University, Harbin 150001, China;

3. Key Laboratory of Micro-systems and Micro-structures Manufacturing, Ministry of Education, Harbin 150001, China)

Abstract: A low-noise closed-loop interface circuit based on a switched-capacitor is presented to improve the noise performance of a MEMS capacitive accelerometer. A charge integrator is adopted as pre-amplifier, which is insensitive to parasitic capacitance and has a very low noise level. The Correlated Double Sampling (CDS) technique is applied to eliminate the $1/f$ noise and the offset of an operational amplifier. Meanwhile, in order to improve dynamic response performance, an integration circuit is introduced to enhance the damping ratio of system and to increase the response speed. The self-test function is also realized by utilizing the same route with charge-discharging. Finally, an elaborate layout design with $0.5\ \mu\text{m}$ CMOS process is completed. The post-simulation results indicate that the sensitivity of the system is $0.115\ \text{V/g}$, nonlinearity is less than 0.12% , minimum acceleration detected can be up to $20\ \mu\text{g}$ and the self-test output is proportional to the self-test voltage.

Key words: accelerometer; closed-loop control; self-test; switched-capacitor; interface circuit

Received date: 2009-01-20; **Revised date:** 2009-04-30.

Foundation item: Supported by the National Hi-Tech Research and Development Program of China (863 Program) (Grant No. 2008AA042201)

1 Introduction

Accelerometers have been popular ever since the safety requirement for automobiles has tightened, especially for seat belts and air-bag systems. This leads to a high demand for low-cost and small-size accelerometers capable of sensing up to $50g^{[1-2]}$. With the development of micro-electromechanical systems (MEMS), closed-loop capacitive MEMS accelerometers meeting the requirements are well received^[3]. In closed-loop accelerometer, the interface circuits limit the overall system resolution. Meanwhile more and more attention is paid to the reliability of MEMS components. One way to improve the reliability is to use a built-in self-test^[4]. So interface circuits with low noise, high stability and self-test function have become important and difficult contents in MEMS accelerometers design. An interface circuit of closed-loop accelerometer whose measurement range is $\pm 50g$ is designed with $0.5 \mu\text{m}$ CMOS process in this paper.

2 Electrical level circuit model for structure

An accelerometer generally consists of a proof-mass suspended by compliant beams anchored to a fixed frame. The proof-mass has a mass of M , the suspended beams have an effective spring constant of K , and there is a damping factor (D) affecting the dynamic movements of the mass^[5]. When affected by external acceleration and electrostatic force, the accelerometer can be modeled by a second mass-damper-spring order system, and the system dynamic equation can be expressed as:

$$M \frac{d^2 x}{dt^2} + D \frac{dx}{dt} + Kx = Ma + F_{\text{SF}}, \quad (1)$$

Where x is the displacement of proof-mass, a is external acceleration and F_{SF} is total electrostatic

force applied to proof-mass. The current equation of an LCR circuit shown in Fig. 1 is expressed as:

$$i_{\text{FB}} + i = C \frac{du}{dt} + Gu + \frac{1}{L} \int u dt = C \frac{d^2 \phi}{dt^2} + G \frac{d\phi}{dt} + \frac{1}{L} \phi. \quad (2)$$

As equation 1 and 2 have the same form, LCR circuit in Fig. 1 can be used as the electrical level model for structure.

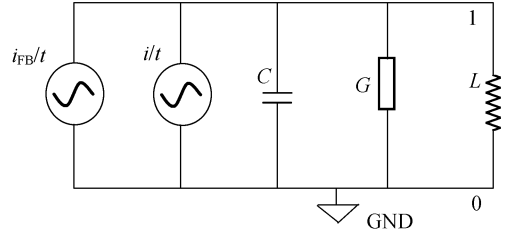


Fig. 1 LCR circuit

3 Circuit design and noise analysis

3.1 Circuit design of closed-loop accelerometer

The switched-capacitor (SC) charge integration method is used for the capacitive sensitivity, owing to the same foundation on which the SC circuit operates, and the sense signal is insensitive to parasitic capacitance and undesirable charging^[6]. The interface circuit is composed of two parts: an analog part which detects the variation of sensing capacitance, obtains output voltages and supplies feedback voltages for sensing elements and a digital part which provides control signals for all switches. In order to compensate finite gain of operational amplifiers, reduce $1/f$ noise and offsets of operational amplifiers, correlated double sampling (CDS) technique is introduced^[7]. Meanwhile, an integration circuit that is used as a closed-loop system controller is added to the system, which enhances the damping ratio of system, increases the speed of response.

In the proof-mass feedback system, self-test is

easy to realize. A self-test voltage is applied to the central electrode. When the voltage is different from the one in balance, the proof-mass will deviate its initial position under electrostatic force effect, equal to an external acceleration. In this design, self-test and charge-discharging adopt the same route, which is controlled by switches-test 1, test 2 and S_5 . When switch test 1 is on and test 2 is off, the system is in the closed-loop feedback mode while S_5 controls charge-discharging to ground. When test 1 is off and test 2 is on, system is in the self-test mode, the self-test voltage is applied to proof-mass through test 2 and S_5 and then the interface circuit detects the variation of sensing capacitance caused by self-test voltages, and exports self-test results. The schematic diagram of the closed-loop accelerometer interface circuit with self-test is show in Fig. 2.

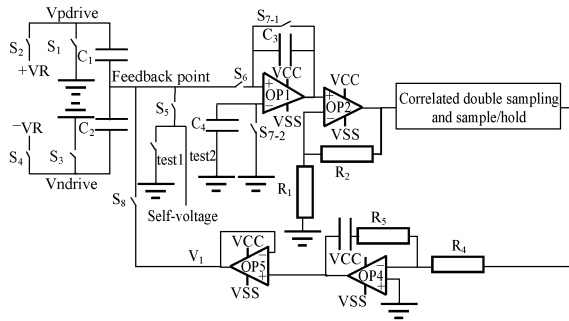


Fig. 2 Schematic diagram of closed-loop accelerometer interface circuit with self-test function

The repetitive cycle of the circuit is $16 \mu\text{s}$ and includes four phases: self-test and sensing phase, detecting phase, sampling phase, and forcing phase. Each cycle starts with the end of forcing period and the beginning of self-test and sensing phase. In the self-test and sensing phase switch S_9 is open, thereby disconnecting the forcing voltage V_f from the central electrode. Very shortly thereafter, switch S_5 is closed which rapidly discharges and brings the

feedback point to ground in normal mode, and in the self-test mode, switch S_5 and test 2 connect the central electrode with the self-test voltage. In the detecting phase, switch S_5 is open and very shortly thereafter, switch S_6 is closed thereby connecting the central electrode to the inverting input of operational amplifier (op amp) OP 1. Then, switches S_{7-1} and S_{7-2} is open, preparing for the charge transference. The charge injected from switch S_{7-1} onto capacitor C_3 is balanced by the charge injected via switch S_{7-2} onto C_4 , thereby providing the first order-cancellation of the parasitic effect at the output of OP1. With the opening of switches S_1 , S_3 and the closing of S_2 , S_4 , a voltage change of V_R occurs on the top plate of C_1 and V_R on the bottom plate of C_2 , the sensing charge is transferred onto the feedback capacitor C_3 , and the output of OP 1 is

$$\frac{-\Delta Q}{C_3} = \frac{V_R(C_1 - C_2)}{C_3}. \quad (3)$$

In the sampling phase, CDS erases the offset of OP 1 and $1/f$ noise, and the sense signal is held at the input of OP 4 via the sample circuit. In the forcing phase, switch S_8 is closed, the output voltage of the sample and hold circuit is applied to the central electrode through the integration circuit. The cycle is repeated at sample rate of the overall system. A well designed op amp can elevate the performance of the whole system, so a low noise op amp is also designed, and all clock pulses are optimized at the same time.

3.2 Layout design of closed-loop accelerometer

The interface circuit is a mixed system, the sensing nodes should be protected from noise sources. Separated analog and digital power supplies are arranged to reduce coupling noises in the digital part. In order to protect weak signals affected by environment noises, all the important weak signals are shielded by guarding rings. The layout area is $4.6 \text{ mm} \times 3.6 \text{ mm}$. An elabo-

rate layout with $0.5\ \mu\text{m}$ CMOS process is shown in Fig. 3.

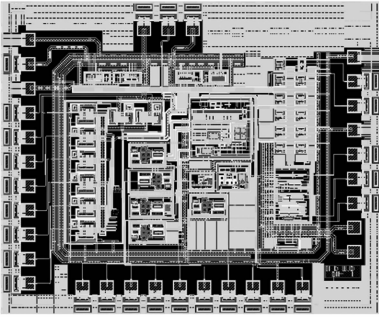


Fig. 3 Layout of closed-loop accelerometer interface circuit

3.3 Noise analysis and optimization

There are several noise sources affecting the overall system resolution of the accelerometer. These noise sources can be mainly classified into two groups: mechanical sources and electrical sources. In the closed-loop accelerometer, the electrical noise dominates the performance of system^[8]. The electronic noise has different components including the front-end amplifier noise, kT/C noise, modulation signal noise and clock jitters noise. The front-end amplifier noise consists of two parts: the thermal noise and $1/f$ noise. Since CDS is employed in the switched-capacitor circuit, $1/f$ noise is reduced remarkably, the thermal noise is the dominant source. The thermal noise is mainly dependent on the integration capacitance values and the sampling frequency^[9-10]. (62.5 kHz sampling frequency and 5 pF integration capacitance are applied to reduce the thermal noise in this design.) kT/C noise is generated by the thermal noise sampling of the switches. This noise is also inversely proportional to the sampling frequency and integration capacitance, and is decreased significantly. Modulation signals and clocks also play important roles, each noise on them directly contributes to the overall noise performance and so, it is important to optimize all clock signals.

4 Results

Simulation and post-simulation are carried out with Hspice. The voltage supplied by power is $\pm 9\ \text{V}$, the simulation results indicate that the full measurement range can be achieved from $-50g$ to $+50g$, the sensitivity of the system is $0.115\ \text{V/g}$, the minimum acceleration detected can be achieved $20\ \mu\text{g}$, nonlinearity is less than 0.12% , and Fig. 4 shows the post-simulation result when input acceleration is $100\ \mu\text{g}$. The relationship between the self-test voltage and the output of system is shown in Fig. 5. The output of system is proportional to the self-test voltage. The output will vary $0.248\ \text{V}$ when the self-test voltage has a change of $1\ \text{V}$, and the equivalent acceleration is $2.36g$.

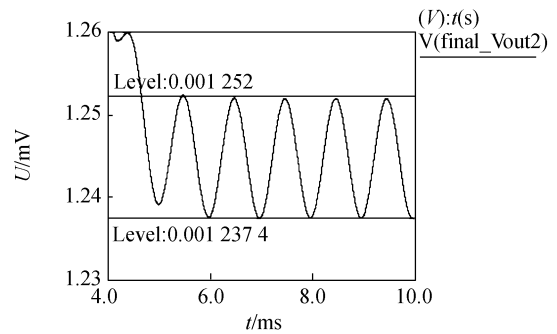


Fig. 4 Post-simulation result of accelerometer when acceleration is $100\ \mu\text{g}$

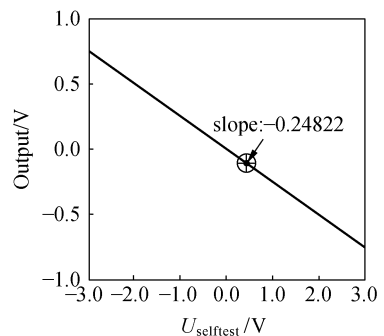


Fig. 5 Relationship between self-test voltage and output of system

5 Conclusions

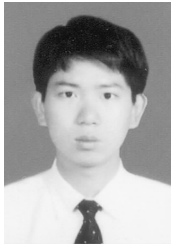
In this research, an interface circuit of closed-loop accelerometer with self-test function is designed and analyzed. SC charge integration, CDS and integration controller are employed to improve its performance and the schematic and

layout design are completed. The postsimulation results indicate that the sensitivity is 0.115 V/g, the minimum acceleration detected can be achieved 20 μ g, and the self-test function is realized. The closed-loop accelerometer can be used in many applications.

References:

- [1] LIU J, QIN L, LIU J CH, *et al.*. A novel differential piezoelectric accelerating sensor [J]. *Opt. Precision Eng.*, 2007, 15(6):903-909. (in Chinese)
- [2] CHE L F, LU Y, XU ZH N. Finite element simulation on packaging of hinged high-g micromachined accelerometer [J]. *Opt. Precision Eng.*, 2007, 15(2):199-205. (in Chinese)
- [3] LEE W F, CHAN P K. A capacitive-based accelerometer IC using injection-nulling switch technique [J]. *IEEE Transactions on Circuits and Systems*, 2008, 55:167-173.
- [4] KUEHNEL W, SHERMAN S. A surface micromachined silicon accelerometer with on-chip detection circuitry [J]. *Sensor and Actuator A*, 1994, 45(1):7-16.
- [5] CHAN K H, LEWIS S R, ZHAO Y. An integrated force-balanced capacitive accelerometer for low-g applications [J]. *Sensor and Actuator A*, 1996, 54(1-3):472-476.
- [6] WU J F, FEDDER G K, CARLEY L R. A low-noise low-offset capacitive sensing amplifier for a 50 μ g/rtHz monolithic CMOS MEMS accelerometer [J]. *IEEE Solid-State Circuits*, 2004, 39(5):722-730.
- [7] TAKAO H, FUKUMOTO H, ISHIDA M. A CMOS integrated three-axis accelerometer fabricated with commercial sub-micrometer CMOS technology and bulk-micromachining [J]. *IEEE Transactions on Electron Devices*, 2001, 48(9):1961-1968.
- [8] HE L, XU Y P. A CMOS readout circuit for SOI resonant accelerometer with 4 μ g bias stability and 20 μ g/rthz resolution [J]. *IEEE Solid-State Circuits*, 2008, 43(6):1480-1490.
- [9] WEL A P, KLUMPERINK E A M. Low-frequency noise phenomena in switched MOSFETs [J]. *IEEE Solid-State Circuits*, 2007, 42(3):541-550.
- [10] ZHANG Y J, CHEN C H, WU B, *et al.*. Structure design of Mach-Zehnder interferometer in electrooptic integrated acceleration seismic geophone [J]. *Opt. Precision Eng.*, 2006, 14(1):77-82. (in Chinese)

Authors' biographies:



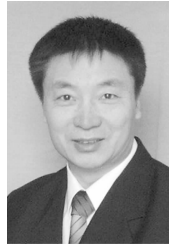
LIU Yun-tao (1980—), male, Ph. D. candidate of the MEMS Center, Harbin Institute of Technology, Harbin Engineering University, his research interests are interface circuits of micro inertial sensors and CMOS analog circuit design. **E-mail:** summer924@sina.com



CHEN Wei-ping (1966—), professor of the MEMS center, Harbin Institute of Technology, his research interests are Micro inertia sensors and micro fluxgate. **E-mail:** chenweiping@hit.edu.cn



YIN Liang (1977—), male, Ph. D. candidate of the MEMS Center, Harbin Institute of Technology, his research interest is CMOS analog circuit design. **E-mail:** yinliang@126.com



WU Qun (1955—), professor of the MEMS center, Harbin Institute of Technology, his research interests are microwave devices and circuits. **E-mail:** qwu@hit.edu.cn

● 下期预告

不同杨氏模量对复合材料储能飞轮应力及位移的影响

李 成¹, 万志超², 郑艳萍¹, 铁 瑛¹

(1. 郑州大学机械工程学院, 河南 郑州 450001; 2. 漯河医学高等专科学校, 河南 漯河 462002)

研究了不同杨氏模量对复合材料飞轮的应力、位移分布的影响。结合复合材料飞轮转子的结构特点, 根据非均质各向异性弹性理论建立了计算模型。得到飞轮在工作转速情况下应力和位移计算的解析公式, 给出了任一点的径向、环向应力及径向位移。并按照所建立的计算模型探讨具有不同杨氏模量的复合材料对径向、环向应力和径向位移的影响。仿真分析了复合材料飞轮转子在不同边界条件、几何参数情况下的应力和位移。结果表明: 随着角速度从 0 增大到 $5\ 000\ \text{s}^{-1}$, 径向应力、环向应力和径向位移同时增大; 两种材料径向应力的最大值都出现在飞轮的外缘, 最大环向应力都出现在飞轮的内侧; 高杨氏模量 ($E_r = 100\ \text{GPa}$, $E_\theta = 350\ \text{GPa}$) 时的径向和环向应力都要大于低杨氏模量时 ($E_r = 20\ \text{GPa}$, $E_\theta = 150\ \text{GPa}$) 的情况。而位移则是在低杨氏模量的情况下较大。